IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method comprising:

at least one of transmitting and receiving a first portion of a first protected data block within a first frame; ~~and~~

at least one of transmitting and receiving a second portion of said first protected data block within a second frame;

calculating an intermediate error checking result based on data in said first portion of said first protected data block;

saving said intermediate error checking result; and

retrieving said intermediate error checking result at the start of said second frame.

2. (Original) The method of claim 1, wherein said first and second frame are in accordance with one of Serial Attached Small Computer System Interface (SAS) protocol and Fibre Channel protocol.

3. (Original) The method of claim 1, wherein said second portion comprises a remaining portion of said first protected block.

4. (Currently Amended) The method of claim 3, further comprising:

~~calculating an intermediate error checking result based on data in said first portion of said first protected data block;~~

~~saving said intermediate error checking result;~~

~~retrieving said intermediate error checking result at the start of said second frame; and~~

calculating a final error checking result in response to, at least in part, said intermediate checking result and data in said remaining portion.

5. (Canceled)

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6. (Currently Amended) The method of claim 1 [[5]], further comprising:

saving an offset value representative of a last data bit of said first portion of said first protected data block; and

continuing, based at least in part upon said offset value and said intermediate error checking result, with an error checking calculation.

7. (Currently amended) An article comprising:

a machine readable medium having stored thereon instructions that when executed by a machine result in the machine performing operations comprising:

at least one of transmitting and receiving a first portion of a first protected data block within a first frame; ~~and~~

at least one of transmitting and receiving a second portion of said first protected data block within a second frame;

calculating an intermediate error checking result based on data in said first portion of said first protected data block;

saving said intermediate error checking result; and

retrieving said intermediate error checking result at the start of said second frame.

8. (Original) The article of claim 7, wherein said first and second frame are in accordance with one of Serial Attached Small Computer System Interface (SAS) protocol and Fibre Channel protocol.

9. (Original) The article of claim 7, wherein said second portion comprises a remaining portion of said first protected block.

10. (Currently Amended) The article of claim 9, wherein said operations further comprise:

~~calculating an intermediate error checking result based on data in said first portion of said first protected data block;~~

~~saving said intermediate error checking result;~~

~~retrieving said intermediate error checking result at the start of said second frame; and~~

calculating a final error checking result in response to, at least in part, said intermediate checking result and data in said remaining portion.

11. (Canceled)

12. (Currently amended) The article of claim 7 ~~11~~, wherein said operations further comprise:

saving an offset value representative of a last data bit of said first portion of said first protected data block; and

continuing, based at least in part upon said offset value and said intermediate error checking result, with an error checking calculation.

13. (Currently amended) A system comprising:

a circuit card comprising circuitry coupled to a bus, said circuitry being capable of, at least one of transmitting and receiving a first portion of a first protected data block within a first frame, and at least one of transmitting and receiving a second portion of said first protected data block within a second frame, wherein said circuitry is capable of calculating an intermediate error checking result in response to data in said first portion of said first protected data block, and said circuitry further being capable of storing said intermediate error checking result in memory and retrieving said intermediate error checking result at a start of said second frame.

14. (Original) The system of claim 13, further comprising:

a circuit board comprising said bus and a bus interface slot, said circuit card being capable of being coupled to said bus interface slot.

15. (Original) The system of claim 14, wherein said circuit card is capable of communicating with at least one device using a communication protocol.

16. (Original) The system of claim 15, wherein said at least one device comprises one or more mass storage devices.

17. (Original) The system of claim 16, wherein said one or more mass storage devices comprise a redundant array of independent disks (RAID).

18. (Original) The system of claim 13, wherein said first and second frame are in accordance with one of Serial Attached Small Computer System Interface (SAS) protocol and Fibre Channel protocol.

19. (Canceled)

20. (Original) A method comprising:

receiving a plurality of sequentially transmitted frames comprising a first and second frame, a first portion of a first protected data block being within said first frame and a second portion of said first protected data block being within said second frame, and at least one of said sequentially transmitted frames is received out of order; and

analyzing a second protected data block of said at least one out of order frame for an error if said second protected data block starts concurrently with said at least one out of order frame.

21. (Original) The method of claim 20, wherein said analyzing comprises calculating at least an intermediate error checking result for said second protected data block.

22. (Currently amended) A partial block communication circuit comprising:

receive circuitry to receive a first portion of a first protected data block within a first frame and to receive a second portion of said first protected data block within a second frame, wherein said circuitry is further capable of calculating an intermediate error checking result based on data in said first portion of said first protected data block, saving said intermediate error checking result, and retrieving said intermediate error checking result at the start of said second frame.

23. (Currently amended) An apparatus comprising:

circuitry capable of at least one of transmitting and receiving a first portion of a first protected data block within a first frame, and at least one of transmitting and receiving a second portion of said first protected data block within a second frame, wherein said circuitry is further capable of calculating an intermediate error checking result based on data in said first portion of said first protected data block, saving said intermediate error checking result, and retrieving said intermediate error checking result at the start of said second frame.

24. (Original) The apparatus of claim 23, wherein said first and second frame are in accordance with one of Serial Attached Small Computer System Interface (SAS) protocol and Fibre Channel protocol.

25. (Original) The apparatus of claim 23, wherein said second portion comprises a remaining portion of said first protected block.

26. (Currently amended) The apparatus of claim 25, wherein said circuitry is further capable of ~~calculating an intermediate error checking result based on data in said first portion of said first protected data block, saving said intermediate error checking result, retrieving said intermediate error checking result at the start of said second frame, and~~ calculating a final error checking result in response to, at least in part, said intermediate checking result and data in said remaining portion.

27. (Canceled)

28. (Currently amended) The apparatus of claim 23 ~~27~~, wherein said circuitry is further capable of saving an offset value representative of a last data bit of said first portion of said first protected data block; and continuing, based at least in part upon said offset value and said intermediate error checking result, with an error checking calculation.